

C. Amendments to the Claims.

1. (Previously Presented) A memory cell, comprising:

a first node for storing a first potential;

5 a second node for storing a second potential;

transistor gates formed from a gate layer; and

a capacitor having plates coupled between the first node and

second node, a portion of at least one plate of the capacitor comprising a

first interconnect wiring formed over the gate layer and includes a plurality

10 of conductive layers that interconnects circuit components of the memory

cell.

2. (Original) The memory cell of claim 1, further comprising:

a first inverter having an input coupled to the first node and an

15 output coupled to the second node; and

a second inverter having an input coupled to the second node

and an output coupled to the first node; wherein

the first node stores a true data value and the second node

stores a complementary data value.

20 3. (Original) The memory cell of claim 1, further including:

a first access transistor coupled to the first node; and

a second access transistor coupled to the second node.

4. (Cancelled)

25 5. (Previously Presented) The memory cell of claim 1, wherein:

the first conductive interconnect wiring includes a bottom  
conducting layer, a dielectric layer formed over the bottom conductive  
layer, and a top conductive layer formed over the dielectric layer, the top  
conducting layer forming at least a portion of the first plate of the  
capacitor.

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6. (Previously Presented) The memory cell of claim 1, further including:  
a second conductive interconnect wiring formed over the first  
conductive interconnect wiring that forms at least a portion of a second  
plate of the capacitor.

5      7. (Original) The memory cell of claim 6, wherein:

the second conductive interconnect wiring comprises titanium;  
the bottom conductive layer comprises titanium nitride; and  
the top conductive layer comprises titanium.

10     8. (Cancelled)

9. (Cancelled)

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